REMARKS

Claims 1-20 stand rejected under 35 USC §103(a) as being unpatentable over Sarrica et al. publication entitled, "Theory and Implementation of LSSD scan ring & STUMPS channel Test and Diagnosis" in view of Rajski, U.S. patent 6,662,327.

Claims 1, 2, 13, 19, and 20 have been amended to more clearly state the invention. Each of the pending claims 1-2, 4-13, and 15-20, as amended, is believed to be in condition for allowance, reconsideration and allowance is respectfully requested.

Sarrica et al. publication discloses a level sensitive scan design (LSSD) including L1 L2 shift register latches (SRLs) test process. A LSSD scan ring with for SRLs is illustrated for tests which require a test control module (TCM) to operate in the LSSD scan mode. STUMPS (Self-Test Using a MISR and a Parallel Shift register sequence generator) channels are connected to the SRLs in a Self-Test Scan mode. A pseudo-random pattern generator (PRPG) and a multiple input signature register (MISR) are connected to the scan channels. In an Array scan mode, certain latches on the TCM are designated as address stepper SRLs, while these SRLs are removed from the chains when array initialization is performed. The address stepper SRLs supply the addresses for the arrays. Self-test scan tests performed with the SRLs configured into STUMPS channels include ABT1 and ABT2. Lateral insertion is illustrated in Figure 6, and is used for finding a SRL with a stuck at fault. Lateral insertion analysis is described as being repeated with scan diagnostics running 255 pseudo-random patterns in self-test scan STUMP mode to find the location of a stuck-at-fault.

Rajski, U.S. patent 6,662,327 discloses a method for clustered pattern

generation that maintains high fault coverage of a circuit under test while it reduces the amount of test data to store by using clusters of correlated test patterns. A test pattern generator stores only a small number of center test vectors which serve as centers of clusters. The generator applies each center test vector to a circuit under test multiple times. However, every time the center vector is shifted into the circuit, some of its positions are complemented. The cluster may have a number of spheres which correspond to test vectors derived with various diffraction probabilities and computed to maximize fault coverage, minimize the total number of clusters, and reduce the test application time. The method also encodes several partially specified center test vectors in scan path using the polarity between scan cells, scan order and waveform generators controlling scan inputs. Column 5, lines 45-66 state:

> FIG. 1 is a flowchart of a method for testing such a circuit according to the invention. A computer program or equivalent device reads the ideal description of a circuit to be tested (30) and computes clusters of test patterns (32). Each cluster consists of a center pattern and a number of other patterns derived from the center pattern by complementing some of its positions. From the test patterns and the ideal circuit description, expected circuit signatures are computed for later comparison against actual signature (34).
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> A tester then tests an actual circuit by applying the clusters of test patterns. The tester, however, does not have to store the clusters. Instead, it stores only the center test patterns, the diffraction probabilities, and an initial seed. In addition, a seed and a polynomial are stored so that a diffractor circuit can reproduce exactly the same sequence of patterns as the ones produced for the ideal circuit. The tester applies the center patterns repeatedly, every time complementing some positions in a pseudorandom manner (36). The process is fully deterministic, i.e. the tester reproduces exactly the same patterns as the ones computed as part of the test of the ideal circuit. The tester also computes the actual signature from the responses of the device under test (38). The actual signature is then compared to the circuit's expected signature (40). If the signatures match, the circuit is declared good; if they do not, the circuit is considered faulty.

Reconsideration and allowance of each of the pending claims 1-20, as

amended, is respectfully requested.

The present invention solves a continuing problem for VLSI testing of how to diagnose an exact location of broken scan chain or chains. When there is low or zero yield, the scan chains are often broken so that the only opportunity to learn and diagnose the root cause of the problem is defect localization based upon scan chain failure data. Other known test applications, such as, Level Sensitive Scan Design (LSSD), Logic Built In Self Test (LBIST), Array Built In Self Test (ABIST), functional, Design-For-Test (DFT) and Design-For-Diagnostics (DFD), all assume the scan chains are operational. The problem of a broken scan chain or chains is usually encountered early in a technology life cycle and diagnostics is critical in improving the fabrication process so that manufacturing yield levels can be quickly achieved. An inability to improve the technology and yield can greatly impact a program or at least severely minimize the revenue that could be realized.

Existing methods and approaches to this problem include dumping megafail data on the tester, Automatic Test Pattern Generation (ATPG) directed at each hypothetical broken latch, voltage and timing sensitive methods, IDDQ walk current measurements, power up/down techniques, and LBIST/ABIST engine based techniques. Significant drawbacks are that the known solutions require very large data volumes, extremely long simulation times, and are not always 100% reliable, and further not one single known method is always successful all the time. This can be attributed to the nature of the particular fault and its manifestation, complex faults, and that faults are not limited to the type of chip area that propagates to system paths of the broken latch

or latches whether it originates from combinational logic or array outputs.

The present invention provides fast and efficient techniques that diagnose defects in broken scan chain or chains and that provide a defect location for Physical Failure Analysis (PFA).

Rapid diagnosis to a location for Physical Failure Analysis (PFA) is needed to understand and correct process anomalies. In these low or zero yield situations, the most common failure is often the scan chain. The LSSD Flush and Scan tests will fail when there is one or more broken scan chains on a device. In these cases, there is no operating region where the scan chains are functional. Since other tests utilize the scan chain to perform device tests, such as disclosed in the cited Sarrica publication and Rajski patent, diagnostics of the broken scan chain or scan chains with hard DC flush and scan fails is extremely limited. Also as the density of VLSI devices continue to increase, their respective scan chains will continue to increase in size proportionally and thus, this problem will become even more severe. Fault simulation/test generation, providing extremely vital tools for diagnosing combinational faults, is very inefficient and ineffective for shift register (SR) diagnostics.

Hence, the present invention provides a solution which speeds broken scan chain diagnostics on the majority of the failing devices to enable timely process corrections and yield improvements.

As taught and claimed by Applicants, the characteristic of deterministic patterns or predetermined LSSD patterns is that each pattern is independent from every other pattern. A pattern consists of a Load, primary inputs (PIs), Clocks, and an Unload

sequence. Devices may have thousands of patterns depending upon the size and structure of the logic. During diagnostics, the failing pattern is identified and fault simulation is performed on the failing pattern, Load, Pls, Clocks, and Unload sequence. The circuit states can be quickly achieved by reviewing and simulating the failing pattern load, any Pls/Clocks, and measures.

Independent claim 1, as amended, recites a method for implementing deterministic based broken scan chain diagnostics in a computer test system connected to a Physical Failure Analysis system comprising the steps of: generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern; utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain; unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to

the Physical Failure Analysis system to localize the physical defect; and responsive to consistent results not being identified, selecting another deterministic test pattern.

Applicants respectfully submit that the present invention is patentable over the references of record. The present invention generates a deterministic pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system with the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern and utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain. Applicants only teach these steps.

Sarrica teaches applying scan clocks, not system clocks, as is taught and claimed by with lateral insertion analysis. Applicants respectfully submit that both the cited Sarrica publication and Rajski patent utilize the scan chain to perform device tests. Applicants respectfully submit that the cited Sarrica publication and Rajski patent do not enable, nor suggest utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective

deterministic values in each of the plurality of latches of each said scan chain, as now recited in the independent claims 1, 13, and 19, as amended.

Applicants respectfully submit that the total teachings of the cited Sarrica publication and Rajski patent fail to achieve or enable the method, apparatus, and computer program product for implementing deterministic based broken scan chain diagnostics, as taught and claimed by Applicants, as recited in independent claims 1, 13, and 19.

Further independent claims 1, 13, and 19, as amended, recites unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results of the identified last switching latch in each scan chain. The references of record including Sarrica et al. and Rajski fail to suggest generating, loading, and unloading testing steps a selected number of times with the deterministic test pattern; and checking for consistent results. Further the steps of checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified with the deterministic test pattern, sending the identified last switching latch in each scan chain to the Physical Failure Analysis system to localize the physical defect are only taught by Applicants. These limitations as recited in independent claims 1, 13, and 19, as amended, are not disclosed or suggested by the combined teachings of Sarrica et al. and Rajski.

Thus, each of the independent claims 1 13, and 19, as amended, is

patentable.

Dependent claims 2, 4-12, 15-18, and 20 respectively depend from patentable claims 1, 13, and 19, further defining the invention. Each of the dependent claims 2, 4-12, 15-18, and 20, as amended, is likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-2, 4-13, and 15-20, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

S-signature by

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